**Listing of Claims:**

Claim 1 (amended): A low pass filter comprising:

a differential amplifier comprising a positive input end, a negative input end, a positive output end and a negative output end;

a first resistive device ~~coupled~~ directly connected between the negative input end and a first node;

a second resistive device ~~coupled~~ directly connected between the positive input end and the first node;

a third resistive device substantially the same as the second resistive device ~~coupled~~ directly connected between the negative input end and a second node;

a fourth resistive device substantially the same as the first resistive device ~~coupled~~ directly connected between the positive input end and the second node;

a first capacitive device ~~coupled~~ directly connected between the negative input end and the positive output end; and

a second capacitive device substantially the same as the first capacitive device ~~coupled~~ directly connected between the positive input end and the negative output end.

Claim 2 (original): The low pass filter of claim 1, further comprising:

a fifth resistive device coupled with the first node;

a sixth resistive device substantially the same as the fifth resistive device coupled with the second node; and

a seventh resistive device coupled between the first node and the second node.

Claim 3 (original): The low pass filter of claim 1, wherein the first resistive device, the

second resistive device, the third resistive device, and the fourth resistive device are adjustable impedance circuits respectively comprising:

a first impedance having a first impedance value;

a first switch device coupled to the first impedance;

a second impedance having a second impedance value; and

a second switch device coupled to the second impedance,

wherein by controlling the switching time of the first switch device and the second switch device, the equivalent impedance of the adjustable impedance circuit can be determined by the first impedance value and the second impedance value.

Claim 4 (original): The low pass filter of claim 3, wherein both the first impedance and the second impedance are resistors.

Claim 5 (original): The low pass filter of claim 3, wherein both the first switch device and the second switch device comprise MOS transistors.

Claim 6 (original): The low pass filter of claim 3, wherein the first switch device comprises a first switch electrically connected between the first impedance and a third node, and a second switch electrically connected between the first impedance and a fourth node, and the second switch device comprises a third switch electrically connected between the second impedance and the third node, and a fourth switch electrically connected between the second impedance and the fourth node.

Claim 7 (original): The low pass filter of claim 4, wherein the first switch device and the second switch device are controlled by complementary control signals.

Claim 8 (original): The low pass filter of claim 7 wherein the equivalent impedance is (T1*R1+T2*R2)/(T1+T2), and T1 is the turn-on time of the first switch device, T2 is the turn-on time of the second switch device, R1 is the first impedance value, and R2 is the second impedance value.

Claim 9 (new): A low pass filter comprising:

a differential amplifier comprising a positive input end, a negative input end, a positive output end and a negative output end;

a first resistive device coupled between the negative input end and a first node;

a second resistive device coupled between the positive input end and the first node;

a third resistive device substantially the same as the second resistive device coupled between the negative input end and a second node;

a fourth resistive device substantially the same as the first resistive device coupled between the positive input end and the second node;

a first capacitive device coupled between the negative input end and the positive output end;

a second capacitive device substantially the same as the first capacitive device coupled between the positive input end and the negative output end ;

wherein the first resistive device, the second resistive device, the third resistive device, and the fourth resistive device are adjustable impedance circuits respectively comprising:

a first impedance having a first impedance value;

a first switch device coupled to the first impedance;

a second impedance having a second impedance value; and

a second switch device coupled to the second impedance, wherein by controlling the switching time of the first switch device and the second switch device, the equivalent impedance of the adjustable impedance circuit can be determined by the first impedance value and the second impedance value.

Claim 10 (new): The low pass filter of claim 9, wherein both the first impedance and the second impedance are resistors.

Claim 11 (new): The low pass filter of claim 9, wherein both the first switch device and the second switch device comprise MOS transistors.

Claim 12 (new): The low pass filter of claim 9, wherein the first switch device comprises a first switch electrically connected between the first impedance and a third node, and a second switch electrically connected between the first impedance and a fourth node, and the second switch device comprises a third switch electrically connected between the second impedance and the third node, and a fourth switch electrically connected between the second impedance and the fourth node.

Claim 13 (new): The low pass filter of claim 10, wherein the first switch device and the second switch device are controlled by complementary control signals.

Claim 14 (new): The low pass filter of claim 13 wherein the equivalent impedance is (T1*R1+T2*R2)/(T1+T2), and T1 is the turn-on time of the first switch device, T2 is the turn-on time of the second switch device, R1 is the first impedance value, and R2 is the second impedance value.

Claim 15 (new): A low pass filter comprising:

a differential amplifier comprising a positive input end, a negative input end, a positive output end and a negative output end;

a first resistive device coupled between the negative input end and a first node;

a second resistive device coupled between the positive input end and the first node;

a third resistive device substantially the same as the second resistive device coupled between the negative input end and a second node;

a fourth resistive device substantially the same as the first resistive device coupled between the positive input end and the second node;

a first capacitive device coupled between the negative input end and the positive output end;

a second capacitive device substantially the same as the first capacitive device coupled between the positive input end and the negative output end;

a fifth resistive device coupled with the first node;

a sixth resistive device substantially the same as the fifth resistive device coupled with the second node; and

a seventh resistive device coupled between the first node and the second node.